APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,071	03/01/2002	Oscar Agazzi	1875.1280001	1409

			EXAMINER
26111	7590	07/10/2006	HO, DUC CHI

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ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 07/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/085,071	AGAZZI ET AL.
	Examiner	Art Unit
	Duc C. Ho	2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _27 April 2006_.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1,5,6,11-13,16,17,19,31,32,37-39,42,49,50 and 57-66_ is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☐ Claim(s) _____ is/are rejected.
7) ☒ Claim(s) _3-4, 7-10, 14-15, 20-30, 33-36, 40-41, 43-48, and 51-56_ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1.   Claims 3-16, 43-50, 59, and 60 are objected to because of the following informalities:

Since all numeral steps in claim 1 have been changed to alphabetical steps Applicant is

suggested to replace the existing numeral steps with alphabetical steps.

    Appropriate correction is required.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
>
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
>
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
>
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
>
> manner in which the invention was made.

3.   This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103©

and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4.   Claims 1, 5-6, 11-13, 16-17, 19, 31-32, 37-39, 42, 49-50, 57-66 are rejected under 35

U.S.C. 103(a) as being unpatentable over Azadet et al. (EP 1006 697 A2- IDS record),

hereinafter referred as Azadet, in view of Staszewski et al. (US 6,587,529), hereinafter referred to as Staszewski.

Regarding claim 1, Azadet discloses parallel signal processing for equalization for fibre channels.

(a) receiving a data signal having a symbol rate (the receiver 100-fig. 3 receives the analog data from the output of the preamplifier 115-fig.1 at a bit rate, for example, 1. 25 Gbps, see 0007);

(b) generating N sampling signals having a first frequency that is lower than the symbol rate, the N sampling signals shifted in phase relative to one another (a digital phase locked loop (DPLL) 325-fig. 3 generates N sampling signals at a frequency of 1/N, for example if N is 10, the signals can be sampled at 1/N or 125MHZ, see 0007-0009);

(c) controlling N analog-to-digital converter (ADC) paths with the N sampling signals to sample the data signal at the phases (the ADC 320-1 to 320-N paths are controlled with the N sampling signals to sample the data signal at 125MHZ, see 0009, and figure 3);

(d) individually adjusting one or more parameters for each of the N ADC paths (each of the N ADC paths can be adjusted with one or more parameters in the error estimation circuits 340-1 through 340-N, gain control circuits 350-1 through 350-N and offset cancellation circuits 360-1 through 360-N, see 0010, and figure 3); *and*

(e) generating a digital representative of the received data signal from samples received from the N ADC paths (the adaptive digital processors 370- 1 through 370-N generate the digital data X1-Xk, see 0011-0012, and figure 3).

Azadet, however, does not teach a portion of step d, in which individually adjusting the N sampling signals to reduce phase errors between the received data signal and each of the N sampling signals in the N ADC paths.

One skill in the art would recognize the advantage of individually adjusting at least a parameter such as timing recovery for each of the N ADC paths in order to reduce phase errors between the received data signal and each of the N sampling signals in the N ADC paths.

Staszewski discloses phase detector architecture for phase error estimating and zero phase restarting. The output signal 220-fig. 4 of the timing recovery circuit 401-fig.4 is applied to the ADC 202-fig.4, and adjusted to reduce phase errors, see col. 9-line 26 to col. 12-line 60.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Azadet with Staszewski.

The suggestion/motivation for doing so would have been to provide a timing recovery signal to the N ADC sampling signals to reduce phase errors between the received data signal and each of the N sampling signals in the N ADC paths.

Therefore, it would have been obvious to combine Azadet with Staszewski to obtain the invention as specified in claim 1.

Regarding claim 5, the receiver of Azadet is capable of individually adjusting for offsets in each of the N ADC paths.

Regarding claim 6, the receiver of Azadet is capable of measuring the offsets in a digital domain and individually adjusting for the offsets in the digital domain for each of the N ADC paths.

Regarding claim 11, the receiver of Azadet is capable of individually adjusting for gain errors in the N-ADC paths (see 0009-0010).

Regarding claim 12, the receiver of Azadet is capable of measuring the gain errors in a digital domain and individually adjusting for the gain errors in the digital domain for each of the N ADC paths.

Regarding claim 13, the receiver of Azadet is capable of measuring the gain errors in an M-path parallel feed-forward equalizer (FFE), where M=N, and individually adjusting one or more FFE gain taps associated with each of the N ADC paths.

Regarding claim 16, please see the rejection of claims 2, 5, and 11, respectively.

Regarding claim 49, the receiver of Azadet includes a feed-forward equalizer 500 (see fig. 4, and fig. 5, and paragraphs 0013, 0015), which could be used as a phase interpolator to individually adjust the N sampling signals.

Regarding claim 50, in Azadet the step of individually adjusting one or more parameters for each of the N ADC paths inherently includes a step of performing an equalization process to compensate for one or more of cross-talk, inter-symbol interference, attenuation, and noise.

Regarding claim 59, the receiver of Azadet is capable of performing one or more digital processes on the samples and generating control signals from the one or more digital processes.

Regarding claim 60, the receiver of Azadet is capable of performing one or more M-path parallel digital processes on the samples, wherein M=kN, and k = 1/s , and s=1, and generating control signals from the one or more M (or N) path parallel digital processes, wherein the control signals are used to perform the individual adjusting step.

Regarding claim 63, this claim has similar limitations as claim 1. Therefore, it is rejected under Azadet-Staszewski for the same reasons set forth in the rejection of claim 1.

Regarding claim 17, Azadet discloses parallel signal processing for equalization for fibre channels.

a receiver input (the receiver 100-fig. 3, see 0009-0012);

an analog-to-digital converter (ADC) array of N ADC paths, wherein N is an integer greater than 1, each the ADC path including an ADC path input coupled to the receiver input (an analog-to-digital converter array (not shown) of N ADC paths from the ADC 320-1 through 320-N coupled to the receiver input of the pre amplifier 115-fig.1);

an M-path DSP coupled to the ADC array, wherein M=kN and k is an integer or a

number in the form of 1/s, where s is an integer (a 370 (1-N) path DSP, fig. 3 including the DSP

370-1 through 370-N coupled to the ADC array, wherein M=kN, and k is 1/s, and s=1);

the M-path DSP having a timing recovery module, wherein the timing recovery module

recovers N sampling clocks from a data signal received at the receiver input, the data signal

having a baud frequency, the N sampling clocks having a first frequency that is N times lower

than the baud frequency, the N sampling clocks being shifted in phase relative to one another,

whereby the timing recovery module provides the N sampling clocks to the N ADC paths to

sample the received signal at the phases (the 370-1 to 370-N path DSP having a reference clock

325-fig. 3 having a baud frequency, for example, at 1.25 Gbps, and the N sampling clocks

having a frequency 1/N, or 125MHZ if N=10, see 0007-0009); *and*

means for individually adjusting one or more parameters for each of the N ADC paths

(each of the N ADC paths can be adjusted with one or more parameters in the error estimation

circuits 340-1 through 340-N, gain control circuits 350-1 through 350-N and offset cancellation

circuits 360-1 through 360-N, see 0010, and figure 3).

Azadet, however, does not teach (1) an ADC array of N-ADC paths, and (2) means for

adjusting each of the N sampling signals to reduce sampling phase errors in the N ADC paths.

For (1) Having a N-ADC paths configured in an array chip is a design choice for solid-

state requirement that offers thermal protection, and other advantages such as high speed

processing, relative low cost circuits, and easy implementation.

At the time of the invention, it would have been obvious to a person of ordinary skill in

the art to combine Azadet with a ADC array of N-ADC paths.

The suggestion/motivation for doing so would have been to provide a design choice for solid-state requirement that offers thermal protection, and other advantages such as high speed processing, relative low cost circuits, and easy implementation.

For (2) One skill in the art would recognize the advantage of individually adjusting at least a parameter such as timing recovery for each of the N ADC paths in order to reduce phase errors between the received data signal and each of the N sampling signals in the N ADC paths.

Staszewski discloses phase detector architecture for phase error estimating and zero phase restarting. The output signal 220-fig. 4 of the timing recovery circuit 401-fig.4 is applied to the ADC 202-fig.4, and adjusted to reduce phase errors, see col. 9-line 26 to col. 12-line 60.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Azadet with Staszewski.

The suggestion/motivation for doing so would have been to provide a timing recovery signal to the N ADC sampling signals to reduce phase errors between the received data signal and each of the N sampling signals in the N ADC paths.

Therefore, it would have been obvious to combine Azadet with Staszewski to obtain the invention as specified in claim 17.

Regarding claim 19, in Azadet the module DPLL 325-fig.3 comprises 1-N timing recovery loops including an output coupled to a corresponding one of the N ADC paths, whereby each of the timing recovery loop determines a sampling phase error in the corresponding one of the N ADC paths and individually adjusts a corresponding one of the N sampling signals to reduce the sampling phase error.

Regarding claim 57, this claim has similar limitations as claim 13. Therefore, it is rejected under Azadet for the same reasons set forth in the rejection of claim 13.

Regarding claims 31-32, these claims have similar limitations as claims 5-6, respectively. Therefore, they are rejected under Azadet for the same reasons set forth in the rejection of claims 5-6.

Regarding claims 37-39, these claims have similar limitations as claims 11-13, respectively. Therefore, they are rejected under Azadet for the same reasons set forth in the rejection of claims 11-13.

Regarding claim 42, this claim has similar limitations as claim 16. Therefore, it is rejected under Azadet for the same reasons set forth in the rejection of claim 16.

Regarding claim 58, this claim has similar limitations as claim 50. Therefore, it is rejected under Azadet for the same reasons set forth in the rejection of claim 50.

Regarding claims 61-62, and 64-66, these claims have similar limitations as claim 17, respectively. Therefore, they are rejected under Azadet-Staszewski for the same reasons set forth in the rejection of claims 17.

Allowable Subject Matter

5.   Claims 3-4, 7-10, 14-15, 20-30, 33-36, 40-41, 43-48, and 51-56 are objected to as being independent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc Ho whose telephone number is (571) 272-3147. The examiner can normally be reached on Monday through Friday from 7:00 am to 3:30 pm.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin, can be reached on (571) 272-3134.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7.   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patent Examiner

Duc Ho

07-03-06